Anjuman Islam Janjira Degree College of Science Murud-Janjira, Raigad-402401 Affiliated to University of Mumbai	
Class: -F.Y.B.Sc. C.S.	**Subject: - : Digital Systems & Architecture**
Semester:- I	**Vertical:- Major(MJ1)**
Exam Event:- Winter2024 (SH)	**Marks: - 30**
Date: - 14/11/2024	**Duration: - 01:00 Hour**

N.B. – 1 – All questions are compulsory.
2 – All questions have internal choice.
3 – Figures to the right indicate full marks.

Q1. Answer the following question. (Any 2 out of 4) **10**

1) Compare and analyze synchronous and asynchronous counters.
2) Illustrate the components and functions of the central processing unit (CPU).
3) Design and apply a logic circuit for the expression (A′·B·C)+(B′·D)+(A·C′), including a truth table.
4) Evaluate and compare computer organization and architecture.

Q2. Answer the following question. (Any 2 out of 4) **10**

1) Define a page replacement algorithm and evaluate its purpose by discussing its different types and providing one example for any type.
2) Analyze and compare CISC and RISC architectures.
3) Evaluate the immediate, register addressing modes used in instruction sets.
4) Illustrate RAID level 1 and RAID level 2 with neat labelled diagram.

Q3. Answer the following question. (Any 2 out of 4) **10**

1) Assess the roles of I/O modules, programmed I/O, and interrupt-driven I/O.
2) Analyze the behavior of a 4-to-1 multiplexer. Provide a detailed description, the circuit diagram, and the truth table.
3) Evaluate the page faults for the following string using the Optimal, LRU, and FIFO methods: 2 3 2 1 5 2 4 5 3 2 5 2(Consider a page frame size of 3.)
4) Illustrate the basic instruction cycle by providing its figure and description.